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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	METHODOLOGY OF QUANTIFICATION OF TRANSMISSION PROBABILITY FOR MINORITY CARRIER COLLECTION IN A SEMICONDUCTOR CHIP

Application Number :

Confirmation Number:

First Named Applicant: Anne Watson

Attorney Docket Number: BUR920040120US1

Art Unit: 2825

Examiner: P. KIK

Search string: (6493850 or 6553542 or 6490709 or 5559060 or 5638286 or 20030074641).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
PK	1	6493850	2002-12-10	Venugopal et al.			
PK	2	6553542	2003-04-22	Ramaswamy et al.			
PK	3	6490709	2002-12-03	Kimura et al.			
PK	4	5559060	1996-09-24	Alsmeier et al.			
PK	5	5638286	1997-06-10	Fujimoto			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
PK	1	20030074641	2003-04-17	Kimura et al.			

Signature Phallaka Kik

Examiner Name	Date
Phallaka Kik	6/23/06

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920040120US1	10/711,143
Applicant(s) A. Watson, et al.	
Filing Date August 27, 2004	**Group Art Unit** 2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

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U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
RC		JP2020039		Japan		abstract	✓	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

RC		SUBSTRATE MODELING AND LUMPED SUBSTRATE RESISTANCE EXTRACTION FOR CMOS ESD/LATCHUP CIRCUIT SIMULATION, T. Li, et al., Coordinated Science Laboratory, Dept. of Electrical and Computer Engineering University of Illionois at Urbana-Champaign, Urbana, IL (1999), 6 pages; 1999 ACM.
RC		BIPOLAR TRANSISTOR ACTION AND TRANSPORT EFFECTS RELATING TO CMOS LATCHUP, G. Krieger, IEEE Transactions on Electron Devices, Vol. ED-34, No. 8, August 1987, pgs. 1719-1728

EXAMINER	DATE CONSIDERED
Phallaka Kik	6/24/06

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920040120US1	10/711,143

Applicant(s): A. Watson, et al.

Filing Date	Group Art Unit
August 27, 2004	2825

U.S. PATENT DOCUMENTS

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U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

RD		PARASITIC LATERAL BIPOLAR TRANSISTORS IN CMOS, L. Deferm, et al., Solid-State Electronics, Vol. 32 No. 2, pgs 103-109, 1989
RD		A NEW ANALYTICAL THREE-DIMENSIONAL MODEL FOR SUBSTRATE RESISTANCE IN CMOS LATCHUP STRUCTURES, M. Chen, et al., IEEE Transactions on Electron Devices, Vol. ED-33 No. 4 pgs. 489-493, April 1986

EXAMINER	DATE CONSIDERED
Phallaka Kik	6/24/2006

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920040120US1	10/711,143
Applicant(s) A. Watson, et al.	
Filing Date August 27, 2004	**Group Art Unit** 2825

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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

PR		STATIC AND TRANSIENT LATCHUP SIMULATION OF VLSI-CMOS WITH AN IMPROVED PHYSICAL DESIGN MODEL, M. Strzempa-Depre, et al., IEEE Transactions on Electron Devices, Vol. ED-34 No. 6, June 1987, pgs 1290-1296
PR		A CMOS MODEL FOR COMPUTER-AIDED CIRCUIT ANALYSIS AND DESIGN, J. W. Roberts, et al., IEEE Journal of Solid-State Circuits, Vol. 24, No. 1, February 1989, pgs 128-138

EXAMINER	Phallaka Kik	DATE CONSIDERED	6/24/2006

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INFORMATION DISCLOSURE CITATION *(Use several sheets if necessary)*	Docket Number (Optional) BUR920040120US1	Application Number 10/711,143
	Applicant(s) A. Watson, et al.	
	Filing Date August 27, 2004	Group Art Unit 2825

U.S. PATENT DOCUMENTS

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		CORRELATING THE CHANNEL, SUBSTRATE, GATE AND MINORITY-CARRIER CURRENTS IN MOSFETs, C. Hu et al., IEEE International, Solid-State Circuits Conference, Digest of Technical Papers February 1983, pgs. 88-90

EXAMINER Phallaka Kik	DATE CONSIDERED 6/24/06

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